

Hardware implementation of the SURF feature detector for 4K 4PPC video stream – a demo

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Abstract—This paper describes a hardware implementation of the Speeded Up Robust Features (SURF) algorithm. The feature detector has been fully implemented in programmable logic resources (FPGA) of a Xilinx Zynq UltraScale+ MPSoC device on the ZCU 104 development board. The system has been adapted to work with a 4K (3840x2160 @ 60 fps) video stream in 4 ppc (pixel per clock) format.

Index Terms—SURF, FPGA, Xilinx Zynq SoC, 4K UHD, 4PPC, real-time video processing

I. INTRODUCTION

The SURF algorithm was proposed in [1] as more efficient alternative to the SIFT (Shift Invariant Feature Transform) method. The solution is characterized by high performance and relatively low computational complexity. The detected features are scale-independent due to the use of a multi-resolution pyramid technique. Also the descriptor is orientation invariant. The metric is calculated by Hessian approximation. SURF is commonly used in applications designed for object recognition, classification or 3D reconstruction.

II. HARDWARE IMPLEMENTATION

Computer vision applications are an important part of autonomous robotic systems. In such solutions, it is essential to provide real-time video processing capabilities. To fulfil this requirement, it was decided to implement SURF in programmable logic (PL) of the Xilinx Zynq UltraScale+ MPSoC (Multi-Processor System on Chip) device. Using SoC architecture allows for further integration with other processing units.

In the presented system only the SURF detector part was implemented, as the descriptor needs to be simplified due to limited resources on the used device. Video stream processing is realized using a parallel-pipeline architecture. Separate units calculate results for every step of the algorithm. This is presented in Fig. 1. Main operations are: conversion to greyscale, integral image calculation, context generation, Hessian metric calculation, non-maxima suppression and feature localization interpolation. The modules work simultaneously and output resulted from one is instantly passed to the next. The algorithm uses 2 image octaves (6 independent scales) which are also processed in parallel.

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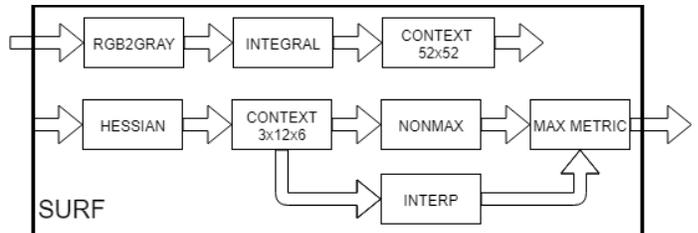


Fig. 1. SURF module architecture

4K resolution is being more and more popular. It is characterized by better image quality but also higher memory usage and higher signal clocking frequency. To avoid the last issue, vector formats were introduced: 2 and 4 ppc (pixel per clock). However, this causes another difficulties. Calculations are done in parallel for each input pixel, which increases logic complexity and utilization of FPGA resources.

III. SUMMARY

The implemented SURF module allows to detect feature points in a ultra high resolution video stream. It uses 2 image octaves and coordinates interpolation. During the design process the correct operation of all modules was confirmed by comparing simulation results with the software model. Finally, real-time image processing for 3840 x 2160 pixels @ 60 fps was achieved. The next step is to add a description calculation unit. The implementation of SURF's original descriptor failed during system development, so we plan to introduce some simplifications. The final purpose of the module is a Structure From Motion application [2]. Our previous design used Harris feature point detector and SAD descriptor on a high definition image (1280 x 720). The use of 4K resolution and a more robust feature point detector and descriptor will improve the performance of the considered system.

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